What is claimed is:

1. A register controlled delayed lock loop for use in a semiconductor memory device, comprising:

a delay line having a plurality of delay cell unit for delaying an non-delayed input clock signal;

a delay model for reflecting a delay condition for an actual clock signal path of the non-delayed input clock signal passing through the delay line;

a delay means for delaying an output signal of the delay model for a predetermined time;

a first phase comparator for comparing a phase of the output signal provided from the delay model with that of the non-delayed input clock signal;

a second phase comparator for comparing a phase of the output signal of the delay means with that of the non-delayed input clock signal;

a mode decision means for determining a continuous execution or termination of an acceleration mode in response to output signals of the first and second phase comparators;

a shift register control means for outputting a left shift signal, a right shift signal and an acceleration shift signal in response to output signals of the first phase comparator and the mode decision means; and

a shift register for controlling a delay value of the delay line in response to an output signal of the shift register control means.

2. The register controlled delayed lock loop as recited in claim 1 wherein a delay value of the delay means is the same to that of the delay line increased in response to the acceleration shift signal

3. The register controlled delayed lock loop as recited in claim 2, wherein the shift register includes:

a plurality of latches, each having a reset terminal, an output terminal and a sub-output terminal;

a plurality of first switches for supplying a value of the latch to a neighboring latch on the left in response to the left shift signal;

a plurality of second switches for supplying a value of the latch to a neighboring latch on the right in response to the right shift signal; and

a plurality of third switches for supplying a value of the latch to another latch separated with a predetermined distance in response to the left shift signal.

4. The register controlled delayed lock loop as recited in claim 1, wherein the mode decision means includes a first latch for latching an output signal of the second phase comparator.

5. The register controlled delayed lock loop as recited in claim 4, wherein the mode decision means includes a second latch for latching the output signal of the mode decision

means.

6. The register controlled delayed lock loop as recited in claim 2, wherein the delay value of the delay means is a multiplication of the delay value of the delay cell unit by a predetermined times.

7. The register controlled delayed lock loop as recited in claim 6, wherein the delay value of the delay means is smaller than a value dividing a frequency of the non-delayed input clock signal.

8. A semiconductor memory device including a delay locked loop, comprising:

a delay line having a plurality of delay cell unit for delaying an non-delayed input clock signal;

a delay model for reflecting a delay condition for an actual clock signal path of the non-delayed input clock signal passing through the delay line;

a delay means for delaying an output signal of the delay model for a predetermined time;

a first phase comparator for comparing a phase of the output signal provided from the delay model with that of the non-delayed input clock signal;

a second phase comparator for comparing a phase of the output signal of the delay means with that of the non-delayed input clock signal;

a mode decision means for determining a continuous execution or termination of an acceleration mode in response to output signals of the first and second phase comparators;

a shift register control means for outputting a left shift signal, a right shift signal and an acceleration shift signal in response to output signals of the first phase comparator and the mode decision means; and

a shift register for controlling a delay value of the delay line in response to an output signal of the shift register control means.

9. The semiconductor memory device of claim 8, wherein a delay value of the delay means is the same to that of the delay line increased in response to the acceleration shift signal

10. The semiconductor memory device of claim 8, wherein the shift register includes:

a plurality of latches, each having a reset terminal, an output terminal and a sub-output terminal;

a plurality of first switches for supplying a value of the latch to a neighboring latch on the left in response to the left shift signal;

a plurality of second switches for supplying a value of the latch to a neighboring latch on the right in response to the right shift signal; and

a plurality of third switches for supplying a value of

the latch to another latch separated with a predetermined distance in response to the left shift signal.

11. The semiconductor memory device of claim 9, wherein the mode decision means includes a first latch for latching an output signal of the second phase comparator.

12. The semiconductor memory device of claim 9, wherein the mode decision means includes a second latch for latching output signal of the mode decision means.

13. The semiconductor memory device of claim 9, wherein the delay value of the delay means is a multiplication of the delay value of the delay cell unit by a predetermined times.

14. The semiconductor memory device of claim 13, wherein the delay value of the delay means is smaller than a value dividing a frequency of the non-delayed input clock signal.

15. The register controlled delayed lock loop as recited in claim 1, further comprising an acceleration mode delay controller for controlling the delay value in the acceleration mode according to operation frequency information.

16. The register controlled delayed lock loop as recited in claim 15, the operation frequency information is generated by using a column address strobe latency (CAS latency).

17. The register controlled delayed lock loop as recited in claim 16, the operation frequency information is generated by using a mode register setting value in case of synchronous semi-conductor memory device.